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10/559,917	12/07/2005	Thomas Rottschafer	DE030203US1	9587

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
NGUYEN, TRONG H	
ART UNIT	PAPER NUMBER
2436	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/559,917	ROTTSCHAFER ET AL.	
	Examiner	Art Unit	
	TRONG NGUYEN	2436	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *1,8,11,16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 04/09/2009 has been entered.

2. The objection to the abstract has been withdrawn due to Applicants' amendment.

The objection to claims **1, 3, 9, 11, 12, 14, 15 and 16** has been withdrawn due to Applicants' amendments.

The rejection of claims **1 and 4** under 35 USC § 112, second paragraph has been withdrawn due to Applicants' amendments.

Response to Arguments

3. With respect to Applicants' argument on page 15 that "the references of record do not disclose, suggest, or teach this subject matter" and that "Matsui does not disclose, suggest, or teach a connection equivalent to the claimed 'intermediate result' line between the control device and the round key generator", the Examiner respectfully disagrees. On Col. 6, lines 4-11, Matsui discloses "First, the input plaintext 3 is **divided** into more significant 4 bytes and less significant 4 bytes, and **the less significant 4 bytes** are **input to** the processing block 9 and **the address calculating circuit 23 through the selector 24**. The address calculating circuit 23 calculates an address of a

extended key to be selected on the basis of the input plaintext data and outputs the calculated address to the extended key latch 7 (Col. 6, lines 4-12)" (emphasis added). Thus, Matsui does disclose a round key generator (i.e. address calculating circuit 23 and magnification key latch 7) using intermediate results (i.e. less significant 4 bytes) received from a control device (i.e. selector 24, selector 25, and step counter 26) in calculating round key.

Claim Objections

4. Claims **1, 8, 11 and 16** are objected to because of the following informalities:

"further" on line 9 of claim **1** should be omitted since only one communication device is being recited in this claim and to provide proper antecedent basis for line 2 of claim **2**.

"adapted to" on line 2 of claim **8** should be "configured to" since language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. See also MPEP § 2111.04.

"the calculated key" on line 16 and "the transferred key" on line 17 of claim **11** should be "the calculated round key" and "the transferred round key" respectively. Moreover, "using" on line 23 should be omitted.

"the data" on line 3 of claim **16** lacks antecedent basis. For examining purposes, hereinafter, "the data" will be interpreted as "the external data".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **1**, **4**, **8**, **9**, **11**, **15**, and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui US 5,261,003 (hereinafter "Matsui") in view of Muratani et al. US 2002/0021802 (hereinafter "Muratani").

Regarding claim **1**, Matsui discloses "**A processor for encrypting and decrypting data comprising:**" as ["a data communication system with a data scrambling" (Col. 5, lines 44-45, Fig. 1)] "**a control device**" [selector 24, selector 25, and step counter 26 (Fig. 1)] "**that receives a data word for encryption or decryption**" as [the less significant 4 bytes are input to the processing block 9 and the address calculating circuit 23 through the selector 24 (Col. 6, lines 4-8)] "**the control device comprising: a memory that temporarily stores an initial key**," as [At the initial state, ….the extended key latch 7 supplies the selected extended key corresponding to the given address to the selector 25, and the key is transmitted to the processing block 9 through the selector 25 (Col. 6, line 2 and 12-15)] "**and at least one external key input that receives the initial key from a source**;" as [At the initial state, …..the magnification key latch 7 supplies the selected extended key to the selector 25

(Col. 6, lines 2 and 12-14, Fig. 1)] "**a round key generator connected to the control device**" as [address calculating circuit 23 and magnification key latch 7 (Fig. 1)] "**via least one further communication device**," as [Fig. 1] "**wherein the round key generator receives the data word from the control device for calculating at least one round key**" as [First, the input plaintext 3 is divided into more significant 4 bytes and less significant 4 bytes, and the less significant 4 bytes are input to the processing block 9 and the address calculating circuit 23 through the selector 24. The address calculating circuit 23 calculates an address of a extended key to be selected on the basis of the input plaintext data and outputs the calculated address to the extended key latch 7 (Col. 6, lines 4-12). *Note that an extended key is generated by calculating its address based on the input plaintext data using the address calculating circuit 23. Thus, the calculated key is a function of the input plaintext. As disclosed by Matsui, since the content of the cipher key or the scramble function to be input to the processing block of each step can be varied depending on the content of the plaintext, high random rate can be obtained and thus the possibility of decoding or analysis of the data communication can be reduced (Col. 9, lines 63-68)*] "**and transfers the at least one round key to the memory of the control deice**;" as [the extended key latch 7 supplies the selected extended key corresponding to the given address to selector 25 (Col. 6, lines 12-14, Fig. 1)] "**and at least one encryption/decryption device**" as [scramble processing means 33 (Fig. 1, Col. 5, line 65)] "**comprising: at least one external data input that receives external data**," as [plaintext 3 (Fig. 1), selector 25 outputs selected extended keys to all of the scramble processing blocks 9-11 in scramble processing

means 33 (Col. 6, lines 14-15, 34-36, Fig. 1)] "**an input that receives the at least one round key from the memory of the control device**," as [selector 25 outputs selected extended keys to all of the scramble processing blocks 9-11 in scramble processing means 33 (Col. 6, lines 14-15, 34-36, Fig. 1)] "**and at least one external data output that outputs data processed with the at least one round key**," as [scrambled text 4 (Fig. 1)] "**wherein the at least one encryption/decryption device and the round key generator communicate solely via the control device**," as [scramble processing means 33 and address calculating circuit 23 and magnification key latch 7 communicate solely using selector 24, selector 25 (Fig. 1)] "**and the control device transmits intermediate results to the round key generator to perform calculation of the at least one round key**" as [First, the input plaintext 3 is **divided** into more significant 4 bytes and less significant 4 bytes, and **the less significant 4 bytes** are **input to** the processing block 9 and **the address calculating circuit 23 through the selector 24**. The address calculating circuit 23 calculates an address of a extended key to be selected on the basis of the input plaintext data and outputs the calculated address to the extended key latch 7 (Col. 6, lines 4-12)]

Matsui does not expressly disclose "**recursive calculation**".

However, Muratani discloses a key generation method wherein round keys are generated recursively on the basis of previous sub keys (Fig. 1).

Muratani and Matsui are analogous art because they are in the same field of endeavor of data encryption/decryption.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Matsui's data communication system with a data scrambling by calculating round key recursively as described by Muratani for the purpose of making it possible to generate expanded keys from the common key in the on-the-fly manner in during encryption and during decoding both without consumption of an unnecessary delay time or storage capacity that has occurred conventionally (Muratani, Col. 14, Par. 0292).

Regarding claim **4**, Matsui in view of Muratani discloses "**The processor of claim 1, wherein the at least one round key is temporarily stored in the memory of the control device**" as [the extended key latch 7 supplies the selected extended key to the selector 25 and the key is then transmitted to the processing block 9 (Matsui, Col. 6, lines 12-15)].

Regarding claim **8**, Matsui in view of Muratani discloses "**The processor of claim 1, wherein the round key generator is adapted to perform a dummy operation**" as [Although exemplary configurations of FIG. 1 and FIG. 2 generate a plurality of expanded keys in number required for the data randomizing section, there can comprise the number of stages for round functions capable of generating expanded keys in number that exceeds the number required for the data randomizing section, wherein a part of the generated expanded keys is used by the data randomizing section (Muratani, Col. 8, Par. 0178). Note that non-used expanded keys are dummy operations as Muratani discloses that a configuration in which only part of the expanded

keys that are capable of being generated is used for data randomizing is effective in view of safety against attack (Muratani, Col. 8, Par. 0185)].

Regarding claim **9**, Matsui in view of Muratani discloses "**The processor of claim 1, wherein a time between the calculating of the at least one round key by the round key generator and the processing of the external data using the at least one round key is variable**" as [Muratani discloses that the order in which the expanded keys are generated may be changed, for example, an earlier generated expanded key may be temporarily stored in a memory to be used later than a later generated expanded key (Fig. 15, Col. 9, Par. 0197, lines 4-5, Par. 0199, lines 1-3)].

Regarding claim **11**, Matsui discloses "**A method of encrypting and/or decrypting data using a processor comprising**:" as [a data communication method with a data scrambling (Col. 4, lines 5-6)] "**reading at least one initial key into a control device**" as [At the initial state, ...the magnification key latch 7 supplies the selected extended key to the selector 25 (Col. 6, lines 2 and 12-14, Fig. 1)] "**reading external data into at least one encryption/decryption device**" as [plaintext 3 (Fig. 1), selector 25 outputs selected extended keys to all of the scramble processing blocks 9-11 in scramble processing means 33 (Col. 6, lines 14-15, 34-36 Fig. 1)] "**reading at least one data word needed to calculate at least one round key from at least one storage device of the control device; transferring the at least one data word to the round key generator**" as [the less significant 4 bytes of plaintext data are input to the address calculating circuit 23 through the selector 24 (Col. 6, lines 6-8)] "**calculating at least one round key on the basis of the at least one data word by using the round**

key generator; transferring the calculated key to the control device; and storing the transferred key in the at least one storage device" as [the address calculating circuit 23 calculates an address of an extended key to be selected on the basis of the input plaintext data and outputs the calculated address to the extended key latch 7 (Col. 6, lines 8-12, Fig. 1) and the extended key latch 7 supplies the selected extended key corresponding to the given address to selector 25 (Col. 6, lines 12-14, Fig. 1). *Note that an extended key is generated by calculating its address based on the input plaintext data using the address calculating circuit 23. Thus, the calculated key is a function of the input plaintext. As disclosed by Matsui, since the content of the cipher key or the scramble function to be input to the processing block of each step can be varied depending on the content of the plaintext, high random rate can be obtained and thus the possibility of decoding or analysis of the data communication can be reduced (Col. 9, lines 63-68)*] "**transferring the at least one round key from the at least one storage device to the at least one encryption/decryption device**" as [selector 25 outputs selected extended keys to scramble processing blocks 9-11 in scramble processing means 33 (Col. 6, lines 14-15, 34-36, Fig. 1)] "**processing the external data by using the at least one encryption/decryption device, using the at least one round key**" as [scramble processing means 3 scrambles an input data by using an extended key to output a scrambled data (Col. 6, lines 15-17, 36-39, Fig. 1)] "**and using the processed data are made available at at least one external data output**," as [scrambled text 4 (Col. 6, lines 44-48, Fig. 1)] "**repeating the method as often as necessary to encrypt or decrypt a set of external data**" as [the same processing as

described above is repeated predetermined times to produce scrambled text 4 (Col. 6, lines 44-48)] "**wherein the control device transmits intermediate results to the round key generator to perform calculation of the at least one round key**" as [First, the input plaintext 3 is **divided** into more significant 4 bytes and less significant 4 bytes, and **the less significant 4 bytes** are **input to** the processing block 9 and **the address calculating circuit 23 through the selector 24**. The address calculating circuit 23 calculates an address of a extended key to be selected on the basis of the input plaintext data and outputs the calculated address to the extended key latch 7 (Col. 6, lines 4-12)].

Matsui does not expressly disclose "**wherein the at least one initial key is obtained from a source other than a round key generator**" and "**round key is calculated recursively**".

However, Muratani discloses an encryption apparatus, decryption apparatus and expanded key generation apparatus and method (Col. 2, Par. 0025, lines 1-3) wherein an initial key (expanded common key kc') is received by a control device (decoder 7 and switching circuit 15) from a source other than a key generation generator (expanded key scheduling section 3) (Fig. 16 and Col. 9, Pars. 0203 and 0204). Moreover, Muratani discloses a key generation method wherein round keys are generated recursively on the basis of previous sub keys (Fig. 1).

Muratani and Matsui are analogous art because they are in the same field of endeavor of data encryption/decryption.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Matsui's data communication system with a data scrambling by having the control device receives an initial key from a source other than the key generation generator and calculating round key recursively as described by Muratani since it would provide for the purpose of being effective in view of safety against attack (Muratani, Col. 8, Par. 0185, line 3 and Col. 9, Par. 0207) and making it possible to generate expanded keys from the common key in the on-the-fly manner during encryption and during decoding both without consumption of an unnecessary delay time or storage capacity that has occurred conventionally (Muratani, Col. 14, Par. 0292).

Regarding claim **15**, this claim contains limitations that are substantially similar to those recited in claim **8** above and accordingly is rejected for the same reasons.

Regarding claim **16**, this claim contains limitations that are substantially similar to those recited in claim **9** above and accordingly is rejected for the same reasons.

7. Claims **2-3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui in view of Muratani and further in view of Frank US 5,255,376 (hereinafter "Frank").

Regarding claim **2**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**wherein the at least one communication device further comprises: first and second request lines; first and second release lines; and first and second data lines**."

However, Frank discloses an improved high speed bus and protocol wherein a bus 10 contains a plurality of request lines, acknowledgement lines, and data lines (Fig. 3).

Frank, Matsui and Muratani are analogous art because they are in the same field of endeavor of computer architecture and data communication.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui in view of Muratani by including at least one communication device comprising a first and second request lines; first and second release lines; and first and second data lines as described by Frank for the purpose of increasing the overall speed of a computer system (Frank, Col. 2, lines 11-15).

Regarding claim **3**, Matsui in view of Muratani and further in view of Frank discloses "**The processor of claim 2**, **wherein the first and second request lines; the first and second release lines; and the first and second data lines at least partially use a single physical path**" as [bus 10 (Frank, Fig. 3, Col. 5, lines 14-27)].

8. Claims **5** and **14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui in view of Muratani and further in view of Tran US 5,919,251 (hereinafter "Tran").

Regarding claim **5**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**wherein the at least one round key is accessed using a rotating pointer**".

However, Tran discloses a rotating pointer buffer for storing data in integrated circuits wherein a head pointer and a tail pointer are used to provide access (Col. 1, lines 51, 54-47, Fig. 1).

Tran, Matsui, and Muratani are analogous art because they are in the same field of endeavor of data storage.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify data communication system with a data scrambling of Matsui in view of Muratani by including at least one rotating pointer to provide access to the selected extended key as described by Tran since rotating pointer structure is superior to shifting structure in terms of lowest area consumption and speed (Tran, Col. 2, lines 18-20, Table 1).

Regarding claim **14**, this claim contains limitations that are substantially similar to those recited in claim **5** above and accordingly is rejected for the same reasons.

9. Claims **6-7** and **12-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui in view of Muratani and further in view of John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, 2nd ed., Morgan Kaufmann, January 1996 (hereinafter "Hennessy and Patterson").

Regarding claim **6**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**wherein the communication between the control device and the at least one encryption/decryption device and between the**

control device and the round key generator is accomplished using at least one handshake protocol".

However, Hennessy and Patterson disclose an asynchronous bus wherein "self-timed, handshaking protocols are used between bus sender and receiver" (Page 499, Par. 2, lines 1-2).

Hennessy and Patterson, Matsui, and Muratani are analogous art because they are in the same field of endeavor of computer architecture and data communication.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui in view of Muratani by using handshaking protocols as described by Hennessy and Patterson since it would be much easier to accommodate a variety of devices and to lengthen the bus without worrying about clock skew or synchronization problems (Hennessy and Patterson, Page 499, Par. 3, lines 1-3).

Regarding claim **7**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**wherein the operation of the of the control device, of the at least one encryption/decryption device, and of the round key generator are asynchronous with respect to one another**".

However, Hennessy and Patterson disclose an asynchronous bus wherein "self-timed, handshaking protocols are used between bus sender and receiver" (Page 499, Par. 2, lines 1-2).

Hennessy and Patterson, Matsui, and Muratani are analogous art because they are in the same field of endeavor of computer architecture and data communication.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui in view of Muratani by including an asynchronous bus as described by Hennessy and Patterson since it would be much easier to accommodate a variety of devices and to lengthen the bus without worrying about clock skew or synchronization problems" (Hennessy and Patterson, Page 499, Par. 3, lines 1-3).

Regarding claim **12**, this claim contains limitations that are substantially similar to those recited in claim **6** above and accordingly is rejected for the same reasons.

Regarding claim **13**, this claim contains limitations that are substantially similar to those recited in claim **7** above and accordingly is rejected for the same reasons.

10. Claims **10** and **17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui in view of Muratani and further in view Verbauwhede US 2003/0202658 (hereinafter "Verbauwhede").

Regarding claim **10**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not disclose "**wherein the processor is an Advanced Encryption Standard (AES) coprocessor**".

However, Verbauwhede discloses AES architecture for encrypting or decrypting data (Col. 1, Par. 0007, line 1).

Verbauwhede, Matsui, and Muratani are analogous art because they are in the same field of endeavor of data encryption/decryption.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui in view of Muratani to be an AES architecture as described by Verbauwhede in order to achieve a high data rate (Verbauwhede, Col. 1, Par. 0006, lines 1-2).

Regarding claim **17**, this claim contains limitations that are substantially similar to those recited in claim **10** above, and accordingly is rejected for the same reasons.

Conclusion

11. Examiner cites particular columns and line numbers in the references as applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG NGUYEN whose telephone number is (571)270-7312. The examiner can normally be reached on Monday through Thursday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NASSER MOAZZAMI can be reached on (571)272-4195. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2436

/T N/
Examiner